

EMIPAK 1B PressFit Power Module 600 V Full Bridge MOSFET, 50 A



EMIPAK 1B
(package example)



RoHS
COMPLIANT

FEATURES

- EF series power MOSFET
- Low input capacitance (C_{iss})
- Ultra low gate charge (Q_g)
- Exposed Al_2O_3 substrate with low thermal resistance
- Avalanche energy rated (UIS)
- Low internal inductance
- Qualified using AQG324 guideline as reference
- PressFit pins locking technology
PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

The EMIPAK 1B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

PRIMARY CHARACTERISTICS	
FULL BRIDGE - QB1 to QB4 MOSFET	
V_{DSS}	600 V
$R_{DS(ON)}$ typical at $I_D = 50$ A	37 m Ω
I_D at $T_{CASE} = 77$ °C	50 A
Type	Modules - MOSFET
Package	EMIPAK 1B
Circuit configuration	Full bridge

ABSOLUTE MAXIMUM RATINGS ($T_J = 25$ °C unless otherwise noted)				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Operating junction temperature	T_J		150	°C
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	$T_J = 25$ °C, all terminals shorted, $f = 50$ Hz, $t = 1$ s	3500	V
QB1 to QB4 - MOSFET				
Drain to source voltage	V_{DSS}		600	V
Gate to source voltage	V_{GS}		± 30	
Pulsed drain current	$I_{DM}^{(1)}$	$V_{GS} = 10$ V	135	A
Continuous drain current	I_D	$T_{SINK} = 25$ °C	44	A
		$T_{SINK} = 80$ °C	34	
Power dissipation	P_D	$T_{SINK} = 25$ °C	173	W
		$T_{SINK} = 80$ °C	97	
Single pulse avalanche energy	E_{AS}	$L = 10$ mH, $I_{AS} = 23$ A, $T_J = 25$ °C	2645	mJ
Pulsed source current (body diode)	I_{SM}		135	A

Note

(1) Pulse width limited by safe operating area

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.



ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
QB1 to QB4 - MOSFET						
Drain to source breakdown voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250 μA	600	-	-	V
V _{DS} temperature coefficient	ΔV _{DSS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.46	-	V/°C
Drain to source on resistance	R _{DSON}	V _{GS} = 10 V, I _D = 50 A	-	37	48	mΩ
		V _{GS} = 10 V, I _D = 50 A, T _J = 150 °C	-	82	-	
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.8	2.7	4.4	V
Temperature coefficient of threshold voltage	ΔV _{GS(th)} /ΔT _J	V _{DS} = V _{GS} , I _D = 250 μA (25 °C to 125 °C)	-	-11.5	-	mV/°C
Forward transconductance	g _{fs}	V _{DS} = 20 V, I _D = 50 A	-	48	-	S
Transfer characteristics	V _{GS}	V _{DS} = 20 V, I _D = 50 A	-	5.3	-	V
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 600 V	-	0.7	10	μA
		V _{GS} = 0 V, V _{DS} = 600 V, T _J = 150 °C	-	1.1	-	mA
Gate to source leakage current	I _{GSS}	V _{GS} = ± 20 V, V _{DS} = 0 V	-	-	± 150	nA
QB1 to QB4 - BODY DIODE						
Source to drain voltage drop	V _{SD}	I _{SD} = 40 A, V _{GS} = 0 V	-	0.92	1.32	V

SWITCHING CHARACTERISTICS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
QB1 to QB4 - MOSFET						
Total gate charge (turn-on)	Q _g	I _D = 50 A, V _{DS} = 480 V, V _{GS} = 10 V	-	240	-	nC
Gate to source charge (turn-on)	Q _{gs}		-	65	-	
Gate to drain charge (turn-on)	Q _{gd}		-	105	-	
Turn-off energy loss	E _{OFF}	I _D = 50 A, V _{DD} = 450 V, V _{GS} = +10 V / -10 V, R _g = 10 Ω, L = 500 μH	-	0.20	-	mJ
Turn-off delay time	t _{d(off)}		-	141	-	ns
Fall time	t _f		-	17	-	
Turn-off energy loss	E _{OFF}	I _D = 50 A, V _{DD} = 450 V, V _{GS} = +10 V / -10 V, R _g = 10 Ω, L = 500 μH, T _J = 125 °C	-	0.24	-	mJ
Turn-off delay time	t _{d(off)}		-	149	-	ns
Fall time	t _f		-	18	-	
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	7500	-	pF
Output capacitance	C _{oss}		-	378	-	
Reverse transfer capacitance	C _{rss}		-	5	-	
Effective output capacitance, energy related	C _{D(er)} ⁽¹⁾	V _{GS} = 0 V, V _{DS} = 0 V to 480 V	-	263	-	pF
Effective output capacitance, time related	C _{D(tr)} ⁽²⁾		-	926	-	
Reverse bias safe operating area	RBSOA	T _J = 150 °C, I _D = 120 A, V _{DD} = 400 V, V _p = 600 V, R _g = 10 Ω, V _{GS} = ± 10 V				
QB1 to QB4 - BODY DIODE						
Diode reverse recovery time	t _{rr}	V _R = 200 V, T _J = 25 °C, I _S = 50 A, dI/dt = 100 A/μs	-	220	-	ns
Diode reverse recovery current	I _{rr}		-	18	-	A
Diode reverse recovery charge	Q _{rr}		-	2000	-	nC

Notes

- (1) C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
- (2) C_{oss(tr)} is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}



INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Resistance	R ₂₅	T _C = 25 °C	5000	Ω
	R ₁₀₀	T _C = 100 °C	493 ± 5 %	
B-value	B _{25/50}	$R_2 = R_{25} \exp. [B_{25/50}(1/T_2 - 1/(298.15K))]$	3375 ± 5 %	K
Maximum operating temperature			220	°C
Dissipation constant			2	mW/°C
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
QB1 to QB4 - MOSFET - Junction to case thermal resistance (per switch)	R _{thJC}	-	-	0.3	°C/W
QB1 to QB4 - MOSFET - Case to sink thermal resistance (per switch)	R _{thCS}	-	0.42	-	°C/W
Case to sink thermal resistance (per module) ⁽¹⁾		-	0.1	-	
Mounting torque (M4)		2	-	3	Nm
Weight		-	28	-	g

Note

⁽¹⁾ Mounting surface flat, smooth, and greased

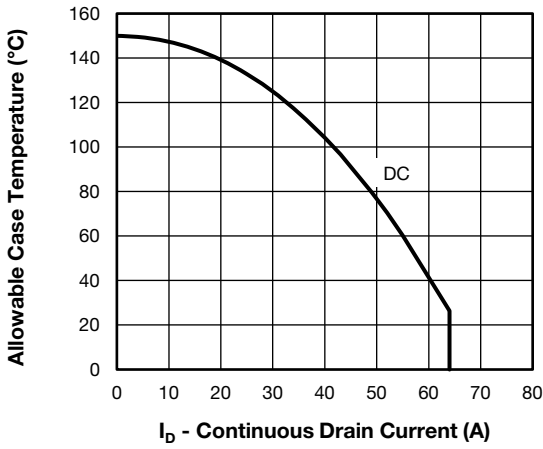


Fig. 1 - Maximum Continuous Drain Current vs. Case Temperature

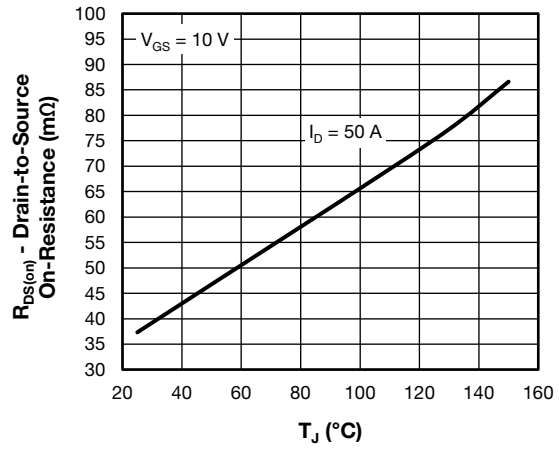


Fig. 4 - Typical Drain to Source On-Resistance vs. Temperature

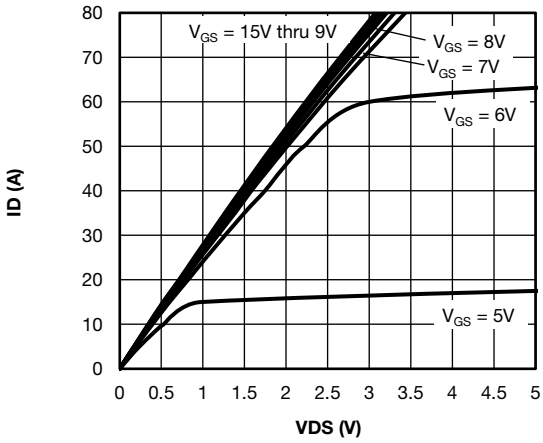


Fig. 2 - Typical Drain to Source Current Output Characteristics at $T_J = 25\text{ }^\circ\text{C}$

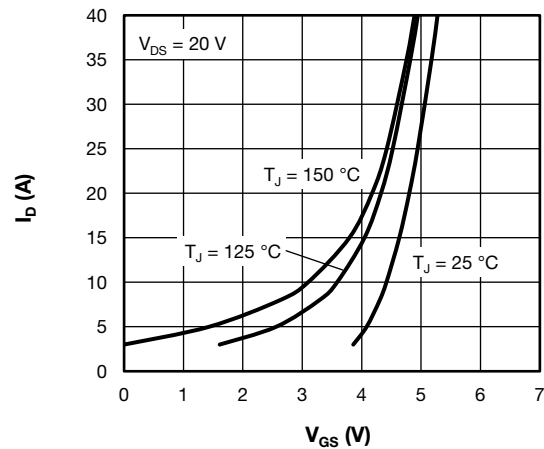


Fig. 5 - Typical Transfer Characteristics

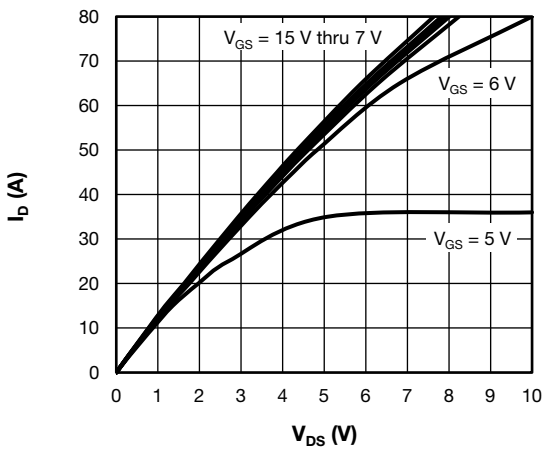


Fig. 3 - Typical Drain to Source Current Output Characteristics at $T_J = 150\text{ }^\circ\text{C}$

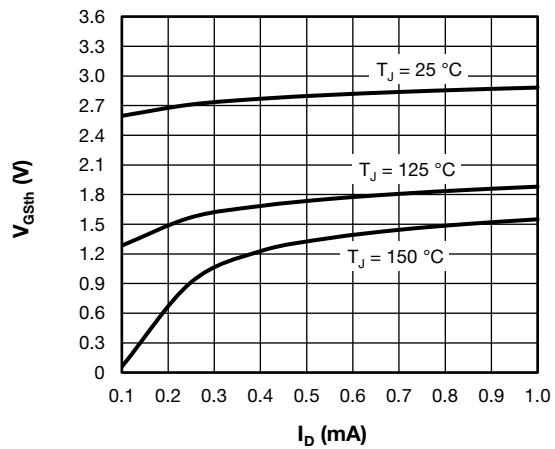


Fig. 6 - Typical Gate Threshold Voltage Characteristics

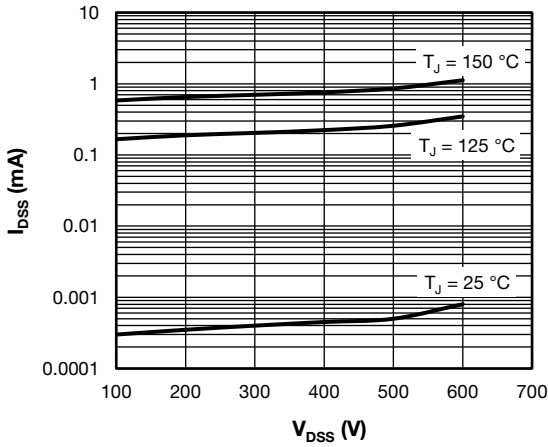


Fig. 7 - Typical Zero Gate Voltage Drain Current

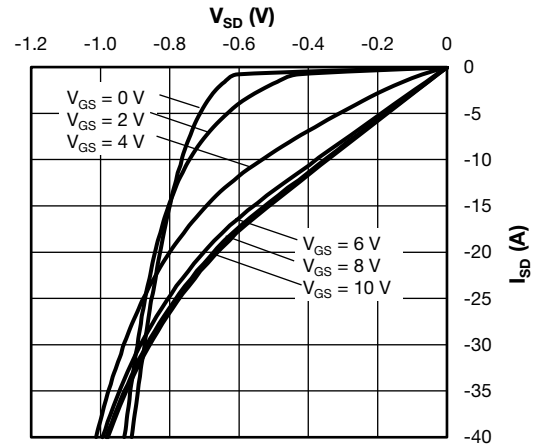


Fig. 10 - Typical Source to Drain Current Characteristics at $T_J = 25^\circ\text{C}$

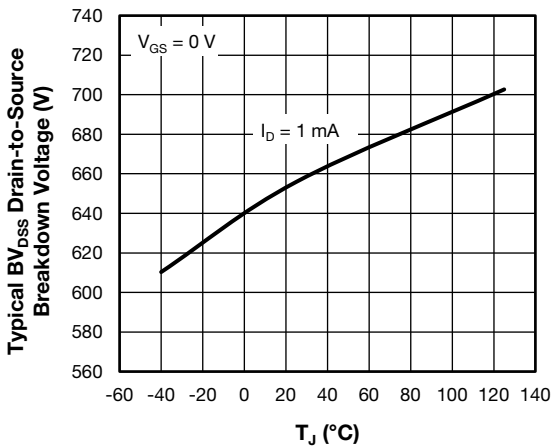


Fig. 8 - Typical Drain to Source Breakdown Voltage vs. Temperature

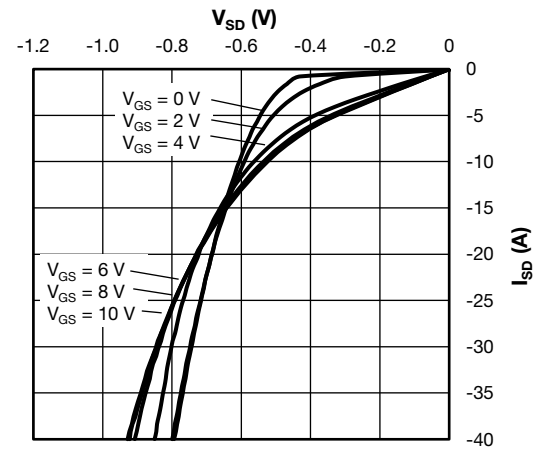


Fig. 11 - Typical Source to Drain Current Characteristics at $T_J = 125^\circ\text{C}$

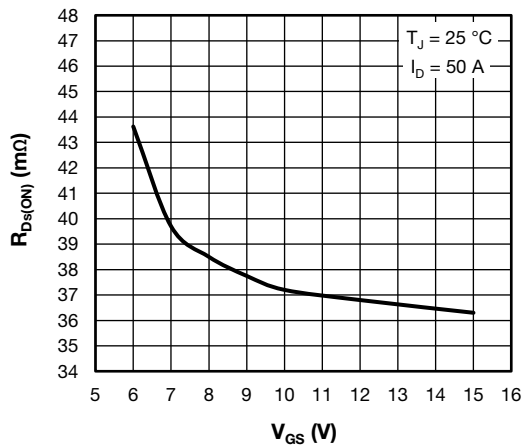


Fig. 9 - Typical Drain-State Resistance vs. Gate to Source Voltage

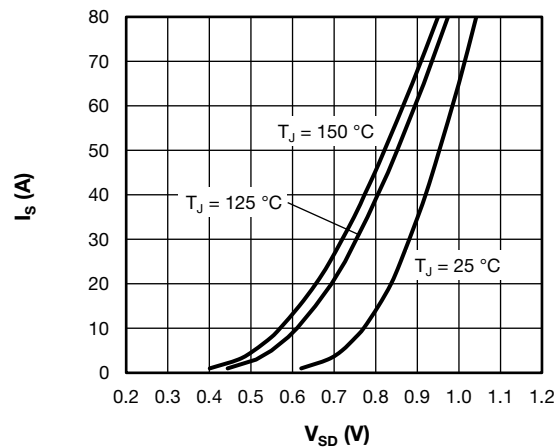


Fig. 12 - Typical Body Diode Source to Drain Current Characteristics

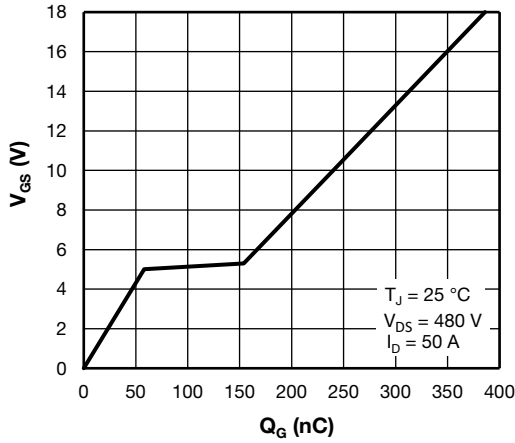


Fig. 13 - Typical Gate Charge vs. Gate to Source Voltage

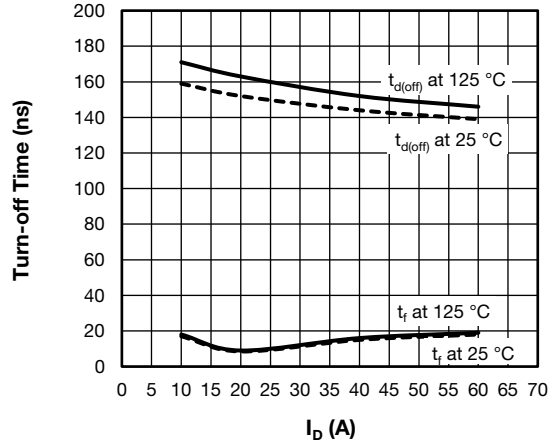


Fig. 16 - Typical Turn-off Switching Time vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\ \Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

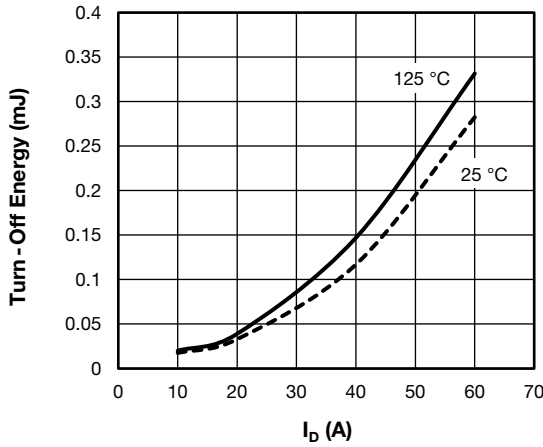


Fig. 14 - Typical Turn-off Energy Loss vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\ \Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

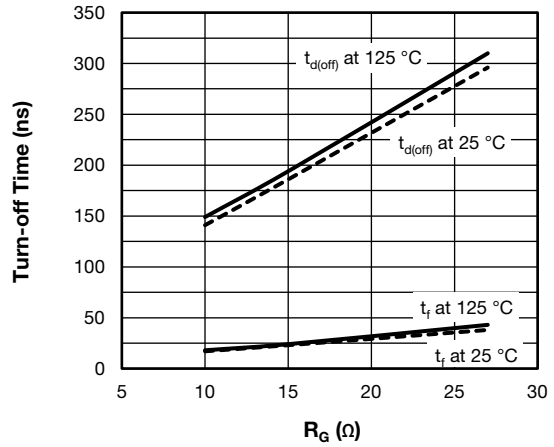


Fig. 17 - Typical Turn-off Switching Time vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 50\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

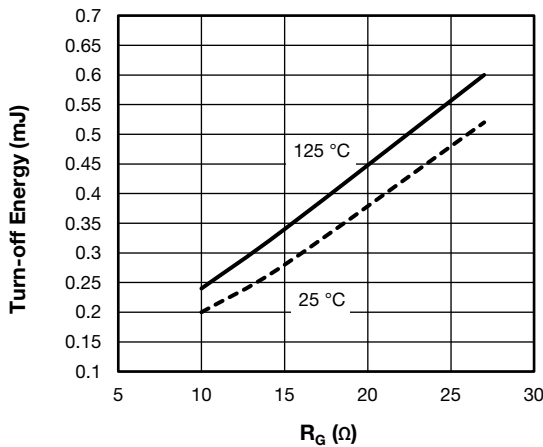


Fig. 15 - Typical Turn-off Energy Loss vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 50\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

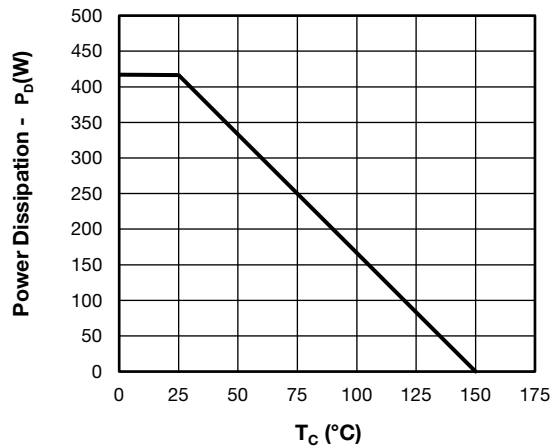


Fig. 18 - Power Dissipation Curve

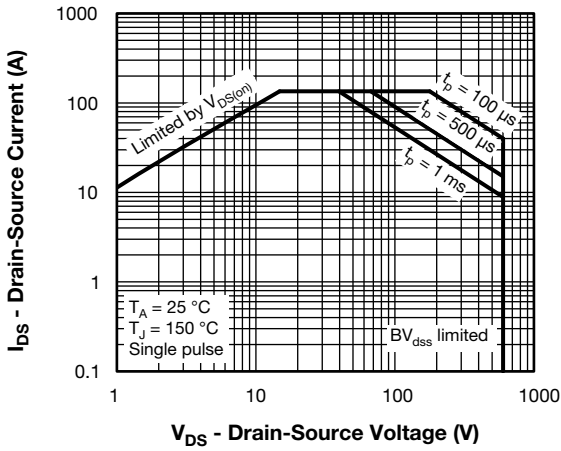


Fig. 19 - Safe Operating Area

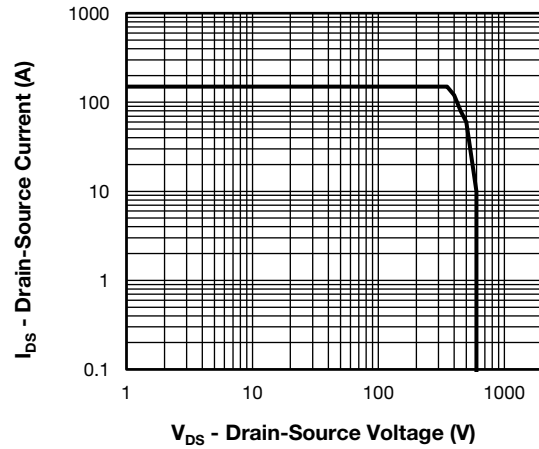


Fig. 20 - Reverse BIAS SOA

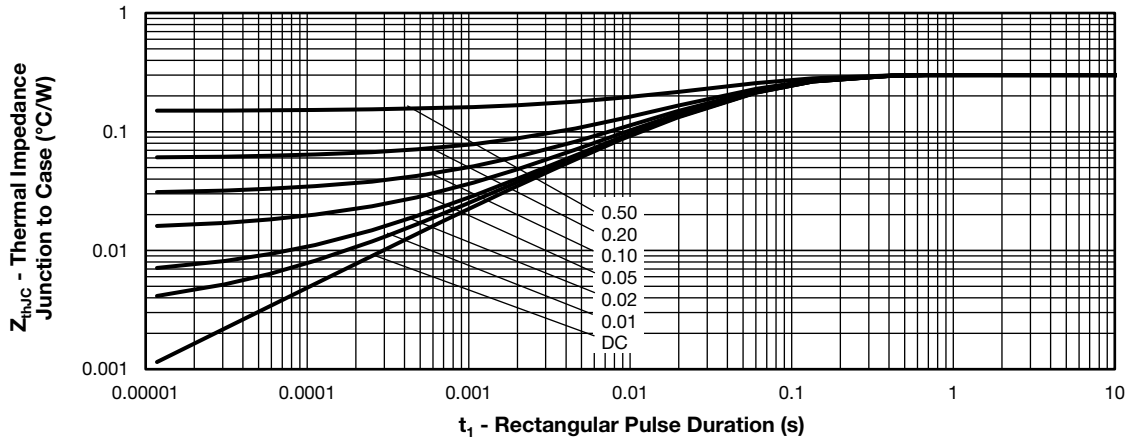
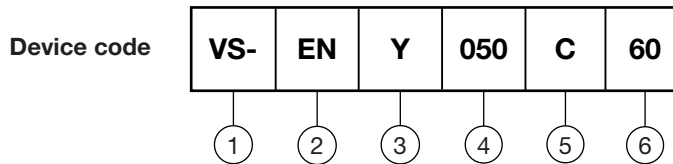


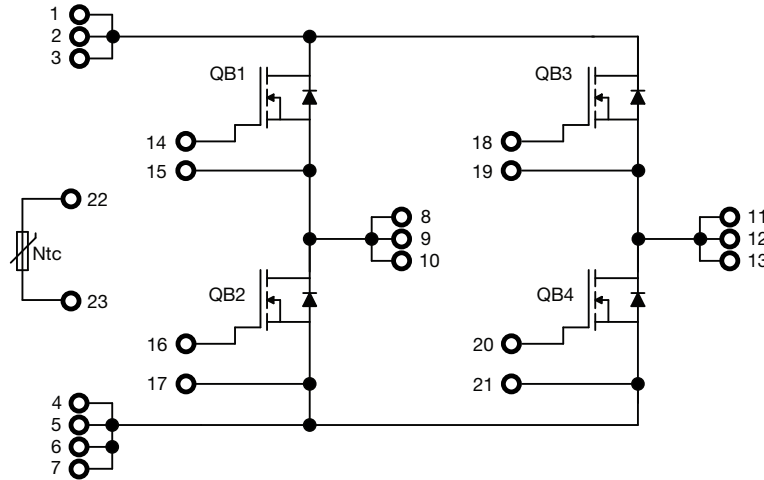
Fig. 21 - Maximum Thermal Impedance Z_{thJC} Characteristics

ORDERING INFORMATION

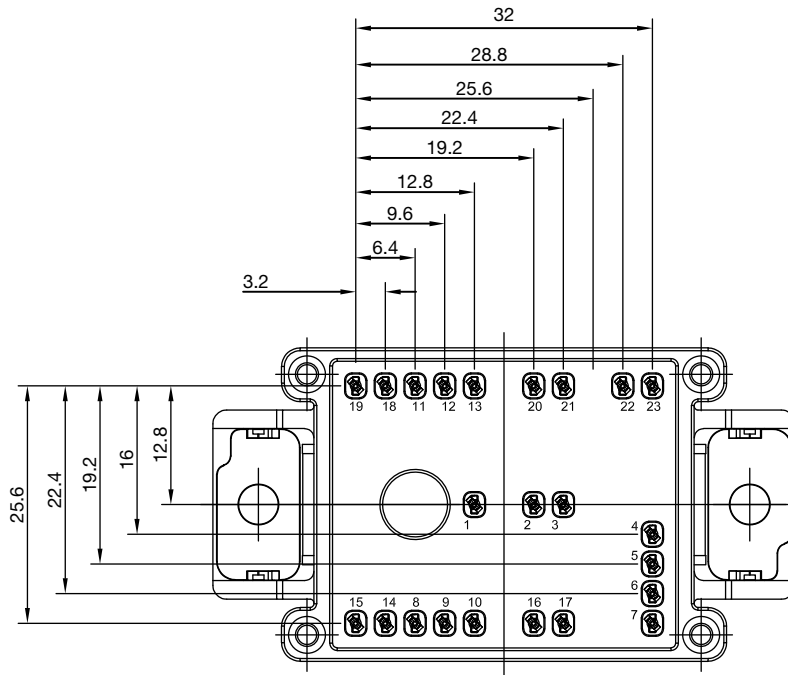


- 1** - Vishay Semiconductors product
- 2** - Package indicator (EN = EMIPAK 1B)
- 3** - Circuit configuration (Y = full bridge topology)
- 4** - Current rating (050 = 50 A)
- 5** - Switch die technology (C = PowerMOS)
- 6** - Voltage rating (60 = 600 V)

CIRCUIT CONFIGURATION



PACKAGE



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95558
Application Note	www.vishay.com/doc?95580



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