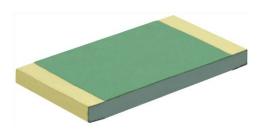
HALOGEN FREE

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(5-2008)



# High Stability - Very High Temperature (270 °C) Thin Film Wraparound Chip Resistors, Sulfur Resistant



#### **DESIGN SUPPORT TOOLS**

click logo to get started



#### INTRODUCTION

For applications such as down hole applications, the need for parts able to withstand very severe conditions (temperature as high as 250 °C powered or up to 270 °C un-powered) has led Vishay Sfernice to push out the limit of the thin film technology.

Designers might read the application note "Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (P, PRA etc...) (High Temperature Application)" www.vishay.com/doc?53047 in conjunction with this datasheet to help them to properly design their board and get the best performances of the PVHT.

Vishay Sfernice research and development engineers will be willing to support any customer design considerations.

#### **FEATURES**

- Operating temperature range: -55 °C; +250 °C
- Storage temperature: -55 °C; +270 °C
- Gold terminations (< 1 µm thick)
- 5 sizes available (0402, 0603, 0805, 1206, 2010); other sizes upon request
- Temperature coefficient down to 5 ppm/°C typical, 10 ppm/°C maximum (-55 °C; +270 °C)
- Tolerance down to 0.05 %
- Load life stability: 0.8 % typical (1 % max.) after 2000 h at 250 °C (ambient) at Pn
- Shelf life stability: 1.5 % typical after 8000 h
- SMD wraparound
- 0.02 % upon request
- TCR remains constant after long term storage at 270 °C
- Sulfur resistant (per ASTM B809-95 humid vapor test)
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912">www.vishav.com/doc?99912</a>

STANDARD ELECTRICAL SPECIFICATIONS						
MODEL	SIZE	$\begin{array}{c} \textbf{RESISTANCE} \\ \textbf{RANGE} \\ \Omega \end{array}$	RATED POWER (1)(2)  P <sub>250 °C</sub> W	LIMITING ELEMENT VOLTAGE V	TOLERANCE ± %	TEMPERATURE COEFFICIENT <sup>(3)</sup> ± ppm/°C
PVHT0402	0402	39 to 45K	0.031	50	0.05, 0.1, 0.5, 1	5, 10, 15, 25, 30, 50, 55
PVHT0603	0603	39 to 108K	0.062	75	0.05, 0.1, 0.5, 1	5, 10, 15, 25, 30, 50, 55
PVHT0805	0805	39 to 240K	0.100	150	0.05, 0.1, 0.5, 1	5, 10, 15, 25, 30, 50, 55
PVHT1206	1206	39 to 900K	0.165	200	0.05, 0.1, 0.5, 1	5, 10, 15, 25, 30, 50, 55
PVHT2010	2010	39 to 2.5M	0.2	300	0.05, 0.1, 0.5, 1	5, 10, 15, 25, 30, 50, 55

#### **Notes**

- (1) For power handling improvement, please refer to application note 53047 "Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (High Temperature Applications)" <a href="https://www.vishay.com/doc?/53047">www.vishay.com/doc?/53047</a> and consult Vishay Sfernice
- (2) See derating curve on next page
- (3) See Table 1 on next page

Revision: 04-Jan-2019

CLIMATIC SPECIFICATIONS				
Operating temperature range	-55 °C; +250 °C			
Storage temperature range	-55 °C; +270 °C			

PERFORMANCE VS. HUMID SULFUR VAPOR				
Test conditions	50 °C ± 2 °C, 85 % ± 4 % RH, exposure time 500 h			
Test results	Resistance drift $<$ (0.05 % $R$ + 0.05 $\Omega$ ), no corrosion products observed			

MECHANICAL SPECIFICATIONS			
Substrate	Alumina		
Resistive Element	Thin Film		
Passivation	Silicon nitride (Si <sub>3</sub> N <sub>4</sub> )		
Protection	Epoxy + Silicone		
Terminations	Gold (< 1 µm) over nickel barrier		

#### Caution:

Performances obtained with following mounting conditions:

- Test board material: alumina
- Solder paste: PbSnAg (93.5/5/1.5)

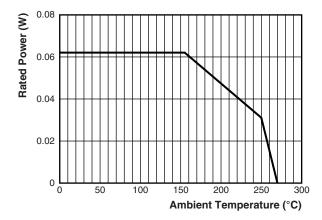
Document Number: 53060



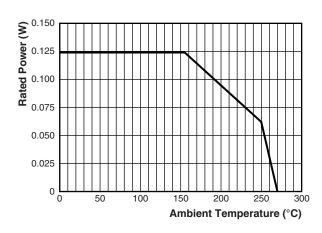
TABLE 1 - TEMPERATURE COEFFICIENT			
7	5 ppm/°C	0 °C; +70 °C	
	10 ppm/°C	-55 °C; +270 °C	
V	10 ppm/°C	-55 °C; +155 °C	
'	15 ppm/°C	-55 °C; +270 °C	
E	25 ppm/°C	-55 °C; +155 °C	
-	30 ppm/°C	-55 °C; +270 °C	
Н	50 ppm/°C	-55 °C; +155 °C	
''	55 ppm/°C	-55 °C; +270 °C	

TABLE 2				
SERIES	RANGE (Ω)	TOL. (± %)	TCR CODE	
0402	39 to < 50	0.1, 0.5, 1	Z; Y; E; H	
0402	50 to 45K	0.05, 0.1, 0.5, 1	Z; Y; E; H	
0603	39 to < 50	0.1, 0.5, 1	Z; Y; E; H	
0603	50 to 108K	0.05, 0.1, 0.5, 1	Z; Y; E; H	
0805	39 to < 50	0.1, 0.5, 1	Z; Y; E; H	
0000	50 to 240K	0.05, 0.1, 0.5, 1	Z; Y; E; H	
1206	39 to < 50	0.1, 0.5, 1	Z; Y; E; H	
1200	50 to 900K	0.05, 0.1, 0.5, 1	Z; Y; E; H	
2010	39 to < 50	0.1, 0.5, 1	Z; Y; E; H	
2010	50 to 2.5M	0.05, 0.1, 0.5, 1	Z; Y; E; H	

#### **POWER DERATING CURVE**

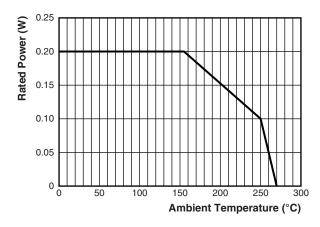


PVHT0402 Power Derating Curve

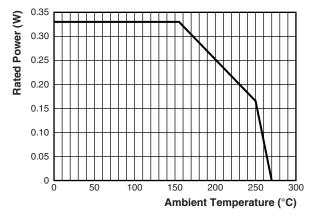


PVHT0603 Power Derating Curve

Revision: 04-Jan-2019

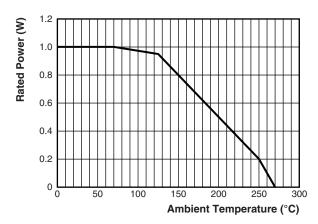


PVHT0805 Power Derating Curve



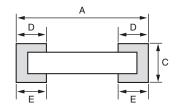
PVHT1206 Power Derating Curve

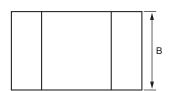




PVHT2010 Power Derating Curve

## **DIMENSIONS** in millimeters (inches)





	Α	В		D/E	
CASE SIZE	MAX. TOL. +0.152 (+0.006) MIN. TOL. -0.152 (-0.006)	MAX. TOL. +0.127 (+0.005) MIN. TOL. -0.127 (-0.005)	С		
	NOMINAL NOMINAL			NOMINAL	TOLERANCE
0402	1.00 (0.039)	0.60 (0.024)		0.25 (0.010)	0.1 (0.004)
0603	1.52 (0.060)	0.85 (0.033)	2 4 (2 2 4 2)	0.38 (0.015)	0.13 (0.005)
0805	1.91 (0.075)	1.27 (0.050)	0.4 (0.016) ± 0.051 (0.002)	0.36 (0.013)	
1206	3.06 (0.120)	1.60 (0.063)	_ = ::::: (0:002)	0.40 (0.016)	0.13 (0.003)
2010	5.08 (0.200)	2.54 (0.100)		0.48 (0.019)	

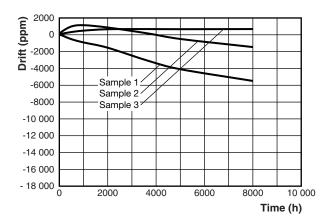
### SUGGESTED LAND PATTERN (TO IPC-7351A)



CHIP SIZE	DIMENSIONS (in millimeter)			
OHIP SIZE	Z <sub>max.</sub>	G <sub>min.</sub>	X <sub>max.</sub>	
0402	1.55	0.15	0.73	
0603	2.37	0.35	0.98	
0805	2.76	0.74	1.40	
1206	3.91	1.85	1.73	
2010	5.93	3.71	2.67	



#### STORAGE CURVE



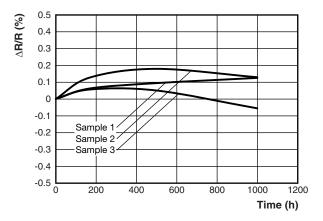
250 °C Drift (Storage) vs. Time

#### **PACKAGING**

ESD packaging available: waffle-pack and plastic tape and reel (low conductivity). Paper tape available upon request (for sizes 0402, 0603, 0805 and 1206).

		NUMBER OF PIE			
SIZE	MOQ	WAFFLE PACK	TAPE AND REEL		TAPE WIDTH
		2" × 2"	MIN.	MAX.	
0402				5000	
0603		100		5000	8 mm
0805	200		100	4000	0 111111
1206		140		4000	
2010		60		1000	8 mm

#### **LOAD LIFE STABILITY CURVES**



PVHT2010: 0.2 W/250 °C

#### Note

 Test performed on samples of 3 different values coming from different lots

#### **PACKAGING RULES**

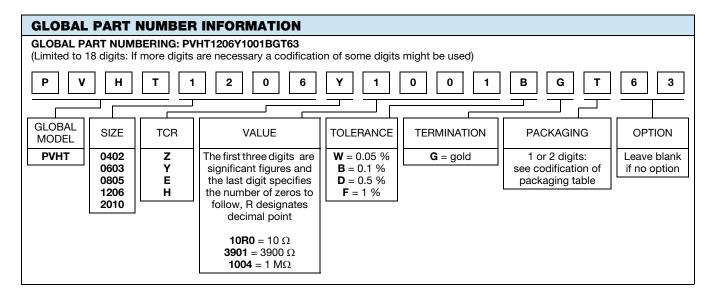
#### **Waffle Pack**

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.

To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code.

#### **Tape and Reel**

See part numbering information to get the quantity desired by tape.







# Vishay Sfernice

CODIFICATION OF PACKAGING				
CODE	PACKAGING			
WAFFLE PACK				
W	100 min., 1 mult			
WA	100 min., 100 mult (available only in size 1206)			
PLASTIC TAPE (standard tape for all sizes)				
Т	100 min., 1 mult			
TA	100 min., 100 mult			
TB	250 min., 250 mult			
TC	500 min., 500 mult			
TD	1000 min., 1000 mult			
TE	2500 min., 2500 mult			
TF	Full tape (quantity depending on size of chips)			
PAPER TAPE (Available for 0402, 0603, 0805 a	nd 1206. Please consult Vishay Sfernice for 2010 size.)			
PT	100 min., 1 mult			
PA	100 min., 100 mult			
PB	250 min., 250 mult			
PC	500 min., 500 mult			
PD (not available for size 0402)	1000 min., 1000 mult			
PE (not available for size 0402)	2500 min., 2500 mult			
PF (not available for size 0402)	Full tape (quantity depending on size of chips)			



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